REMARKS

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The title is amended to read "DIGITAL VIDEO STORAGE SYSTEM FOR STORING AUDIO AND VIDEO BLOCKS RECEIVED FROM INCOMING BIT-STREAM INTO MEMORY AND RELATED METHOD THEREOF". No new matter is entered. As the new title is both descriptive and clearly indicative of the invention to which the claims are directed, applicant respectfully requests withdrawal of the objection to the title.

Correcting of informalities in the claims

Claims 1 and 12 have been amended to more clearly define the claimed DV storage system and method. Support can be found in original Claims 4 and 16. No new matter is entered.

Claims 9-11 are amended to change the term "memory manager" to "buffer manager" as this was the term introduced earlier in claim 4. In this way, antecedent basis problems of claims 9-11 are corrected. No new matter is entered.

Claims 6, 7, 8, 9, 10, 18, 19, 20, 21, 22 are amended to change the indefinite word "if" to the definite word "when". No new matter is entered.

Claims 21 and 22 are amended to change the term "data extractor" to "DV demuxer" as this was the term introduced earlier in claim 16. In this way, antecedent basis problems of claims 21 and 22 are corrected. No new matter is entered.

Claim 15 has been amended to correct typographical errors. No new matter is entered.

Claims 12, 13 are rejected under 35 USC 102e as being anticipated by Hoshi et al (US 7,197,231 B2)

Applicant asserts that claims 12 and 13 should not be found anticipated by Hoshi et al.

because Hoshi et al. do not teach each and every limitation of the present invention as claimed.

A first difference between the present invention and Hoshi et al. is that Hoshi et al. do not teach or suggest directly receiving the incoming bit-stream from the interface module. As is shown in Figure 1 by Hoshi et al., the tuner unit 101 is separated from the demultiplexer 103 by the descrambler 102. Therefore, the incoming bit-stream is not directly received from the interface module as is claimed in the present invention because the descrambler 103 is in the way. This is also true in the VTR unit 200 of Figure 1. Mainly, the tuner unit 201 is separated from the demultiplexer 203 by the descrambler 202. For this reason, applicant asserts that Hoshi et al. do not teach "directly receiving the incoming bit-stream from the interface module", as is claimed in claim 12 of the present invention.

A second difference between the present invention and Hoshi et al. is that Hoshi et al. do not teach or suggest storing the video blocks and audio blocks in a memory. In the Office action of 09/27/2007, the Examiner stated that this features is taught by Hoshi et al. because "figure 1, Recording circuit 216 and 217 in the VTR unit 200". However, the applicant respectfully disagrees. The reason is that the recording processing circuits 216, 271 are not the same as a memory. In particular, the processing circuit 216 is described in col 5, lines 27-33 as "The recording / reproducing processing circuit 216 performs processing necessary for recording, such as synchronization, addition of IDs and the like, error-correcting encoding, digital modulation and the like, for the image data D1 and the sound data D2 input from the demultiplexer 203, and outputs resultant data to a recording / reproducing circuit 217." Applicant notes that "synchronization, addition of IDs and the like, error-correcting encoding, digital modulation and the like" is not equivalent or similar to "storing the video blocks and audio blocks in a memory", as is claimed in claim 12 of the present invention. In the present invention, the video blocks and audio blocks output by the demultiplexer are stored in a memory; however, in the teachings of Hoshi et al. processing is first performed on the image data D1 and the sound data D2 by the processing circuit 216 to thereby produce "resultant data". The resultant data is then recorded on a magnetic tape. See col 5, lines 34-36 stating,

"The recording/reproducing circuit 217 records the image data and the sound data input from the recording / reproducing processing circuit 216 on a magnetic tape." The applicant asserts that this functionality is not the same as is claimed by the present invention because the audio and video blocks are not stored in a memory as in the present invention, but are instead first processed to form resultant data which is then stored on a magnetic tape. In other words, the method operation of Hoshi et al. is not the same as is claimed in the present invention.

Further, Hoshi et al. do not teach or suggest checking the incoming bit-stream for errors. Applicant respectfully submits that Examiner admitted that Hoshi et al, Okamori and Tan et al fail to teach this feature in page 7 of the Office action of 09/27/2007. However, Examiner further stated Xue et al teach this feature in column 2, lines 9-36 and column 2. Applicant respectfully disagrees. In particular, the cited paragraph of Xue states "Once the first receive buffer is full, the receiving device stores subsequent CIP packets 20 in a second receive buffer. Hardware and/or software concurrently processes the CIP packet sequence in the first receive buffer to reconstruct data contained therein in accordance with a format expected by an application program". Applicant notes that Xue reconstructs data contained in a received stream in accordance with an expected format, which is not equivalent or similar to "checking the incoming bit-stream for errors", as is claimed in amended claim 12 of the present application. As described in paragraphs 32 and 33 in the present application, DV demuxer checks the incoming bit-stream DV_DATA for errors to determine if the incoming bit-stream DV_DATA is compliant with the DV format. In contrast, Xue merely describes constructing data in a received stream in accordance with an expected format. Xue does not mention "anything about checking the incoming bit stream for errors". For this reason, applicant asserts that neither Xue nor Hoshi et al. teach "checking the incoming bit-stream for errors", as is claimed in claim 12 of the present invention.

For at least the above stated reasons, applicant asserts that claim 12 should not be found rejected under 35 USC 102e as being anticipated by Hoshi et al. Claims 13-23 are dependent claims being dependent upon claim 12 and should therefore be allowed for at least the same

reasons. Reconsideration of claims 12-23 is respectfully requested.

Claims 1, 2 are rejected under 35 USC 103a as being unpatentable over Hoshi et al (US 7,197,231 B2) as applied to claim 12 above, and further in view of Ihara (US 7, 199,891 B1)

Applicant asserts that claims 1 and 2 should not be found unpatentable as being obvious in view of Hoshi et al. in combination with Ihara because neither Hoshi et al. nor Ihara teach all the limitations of the present invention and the differences would not be obvious to a person of ordinary skill in the art without further inventive process.

Similar to as mentioned above for the rejection of claim 12, a first difference between the present invention and the teachings of Hoshi et al. and Ihara is that Hoshi et al. and Ihara do not teach or suggest "a DV demuxer directly connected to the interface module for receiving the incoming bit-stream", as is claimed in claim 1 of the present invention. As is shown in Figure 1 by Hoshi et al., the tuner unit 101 is separated from the demultiplexer 103 by the descrambler 102. Therefore, the incoming bit-stream is not directly connected to the descrambler as is claimed in the present invention because the descrambler 103 is in the way. This is also true in the VTR unit 200 of Figure 1 by Hoshi et al. and also in Figure 2 of Ihara showing the demodulator 11 being separated from the demultiplexer 14 by both the descrambling unit 12 and the data conversion 13.

A second difference between the present invention and Hoshi et al. and Ihara is that neither Hoshi et al. nor Ihara teach or suggest "a memory coupled to the DV demuxer for storing the video blocks and audio blocks", as is claimed in claim 1 of the present invention. In the Office action of 09/27/2007, the Examiner stated that this features is failed to by taught by Hoshi et al. but it is taught by Ihara because "figure 2, memory 15 is coupled to the de-multiplexer 14, column 5, line 56-column 6, line2)". However, the applicant respectfully disagrees. The reason applicant disagrees is that the memory 15 of Ihara is "video memory" and is not for storing the video blocks and audio blocks as is claimed in claim 1. In particular, the memory 15 of Ihara is only for storing video data. In particular, applicant notes that col 7,

lines 57-62 state, "The demultiplexer 14 is fed from the MPEG processor 16 with still image data, composed of the luminance information and the chroma information, under control by the CPU 23, and stores the still image data in the image memory 15 to output the stored data to the data conversion unit 13 under control by the CPU 23." Additionally, col 17, lines 24-26 of Ihara state, "This causes the CPU 23 to store the still image data composed of the luminance information Y and the chroma information Cr, Cb in the image memory 15." Applicant notes that such functionality is completely different than that of the present invention. In the present invention, both audio blocks and video blocks de-multiplexed from the received blocks in the incoming bit-stream are stored in the memory. Applicant asserts that it would not be obvious to a person of ordinary skill in the art to also store audio blocks in the video memory 15 of Ihara because Ihara's invention has nothing to do with audio. Ihara is solely focused on image processing – see the title of Ihara stating, "Image processing method and apparatus, printing method and apparatus, image printing system and method and recording medium". Applicant asserts that there would be no motivation for a person skilled in the art to combine anything related to audio processing to Ihara because Ihara would not be benefited by storing audio information. For this reason, applicant asserts that it would not be "obvious to try" as was stated by the Examiner in the current Office action. In particular, it would not be obvious to try because the video memory 15 of Ihara would be understood by a person skilled in the art to have nothing to do with audio blocks.

Further, similar to as mentioned above for the rejection of claim 12, Hoshi et al. and Ihara do not teach or suggest "a DV demuxer directly connected to the interface module for receiving the incoming bit-stream, wherein the DV demuxer **checks the incoming bit-stream for errors** and de-multiplexes received blocks in the incoming bit-stream into at least video blocks being in video sections and audio blocks being in audio sections" (emphasis added). Applicant respectfully submits that Examiner admitted that Hoshi et al, and Ihara fail to teach this feature in the Office action of 09/27/2007. Even though Examiner further stated Xue et al teach this feature in column 2, lines 9-36 and column 2, Applicant respectfully disagrees. The cited paragraph of Xue merely describes constructing data in a

received stream in accordance with an expected format, which is not equivalent or similar to "checking the incoming bit-stream for errors", as is claimed in amended claim 1 of the present application. For this reason, applicant asserts that neither Xue, nor Ihara and Hoshi et al. teach "a DV demuxer directly connected to the interface module for receiving the incoming bit-stream, wherein the DV demuxer **checks the incoming bit-stream for errors** and de-multiplexes received blocks in the incoming bit-stream into at least video blocks being in video sections and audio blocks being in audio sections", as is claimed in claim 1 of the present invention.

For at least the above stated reasons, applicant asserts that claim 1 should not be found rejected under 35 USC 103a in view of Hoshi et al. and Ihara. Claims 2-11 are dependent claims being dependent upon claim 1 and should therefore be allowed for at least the same reasons. Reconsideration of claims 1-11 is respectfully requested.

Claim 3 is rejected under 35 USC 103a as being unpatentable over Hoshi et al (US 7,197,231 B2) and Ihara (US 7,199,891 B1) as applied to claims 1, 2 above, and further in view of Okamori (US 2003/0,053,486 A1) and Tan et al (US 5,959,684)

As previously mentioned, claim 3 is dependent upon base claim 1 and should therefore be found allowable for at least the same reasons as provided above for the base claim. Reconsideration of claim 3 is respectfully requested.

Claims 4, 5, and 11 are rejected under 35 USC 103a as being unpatentable over Hoshi et al (US 7,197,231 B2), Ihara (US 7,199,891 B1) and Okamori (US 2003/053/486 A1) and Tan et al (US 5,959,684) and further in view of Xue et al (US 6,711,181 B1)

As previously mentioned, claims 4, 5, and 11 are dependent upon base claim 1 and should therefore be found allowable for at least the same reasons as provided above for the base claim. Reconsideration of claims 4, 5, and 11 is respectfully requested.

Claims 14 and 15 are rejected under 35 USC 103a as being unpatentable over Hoshi et al (US 7,197,231 B2) as applied to claims 12, 13 above, and further in view of Okamori (US 2003/053/486 A1) and Tan et al (US 5,959,684)

As previously mentioned, claims 14 and 15 are dependent upon base claim 12 and should therefore be found allowable for at least the same reasons as provided above for the base claim. Reconsideration of claims 14 and 15 is respectfully requested.

Claims 16, 17, 23 are rejected under 35 USC 103a as being unpatentable over Hoshi et al (US 7,197,231 B2), Ihara (US 7,199,891 B1) and Okamori (US 2003/053/486 A1) and Tan et al (US 5,959,684), and further in view of Xue et al (US 6,711,181 B1)

As previously mentioned, claims 16, 17, and 23 are dependent upon base claim 12 and should therefore be found allowable for at least the same reasons as provided above for the base claim. Reconsideration of claims 16, 17, and 23 is respectfully requested.

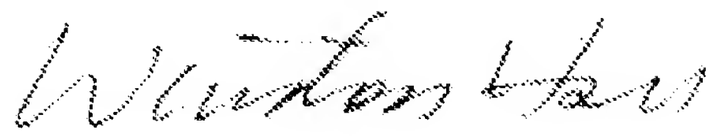
Allowable subject matter – Claims 6-10 and 18-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant thanks the Examiner for the allowance of claims 6-10 and 18-22. Because the applicant believes the base claims 1 and 12 should not be found rejected for the above stated reasons, applicant has not rewritten claims in 6-10 and 18-22 in independent form.

Conclusion:

Thus, all pending claims are submitted to be in condition for allowance with respect to the cited art for at least the reasons presented above. The Examiner is encouraged to telephone the undersigned if there are informalities that can be resolved in a phone conversation, or if the Examiner has any ideas or suggestions for further advancing the prosecution of this case.

Sincerely yours,



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